Integrated TFT Panel Power Supply with Gate Modulation and VCOM

Preliminary Technical Data

ADD8733

FEATURES

- **Step-up switching regulator with 3 A switch current limit**
  - **8 V to 16.5 V input voltage range**
  - **Adjustable output voltage up to 20 V**
  - **1.2 A series switch for power sequencing**
  - **Overvoltage protection (OVP)**
- **Step-down switching regulator with 3 A switch current limit**
  - **8 V to 16.5 V input voltage range**
  - **Adjustable output voltage down to 2.5 V**
- **Gate pulse modulator circuitry**
  - **Independently adjustable delay and falling slope**
- **Positive charge-pump regulator for VGH**
- **Negative charge-pump regulator for VGL**
- **Two VCOM amplifiers**
- **General**
  - **Power supply sequencing**
  - **Thermal fault protection**
  - **650 kHz or 1.2 MHz PWM frequency**
  - **Soft start**
  - **Undervoltage lockout (UVLO)**
  - **48-lead RoHS compliant LFCSP**

APPLICATIONS

TFT LCD panels for TVs and monitors

BLOCK DIAGRAM

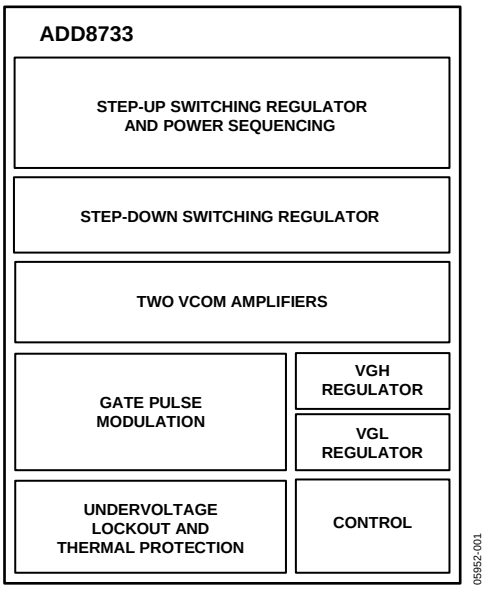

Figure 1.

GENERAL DESCRIPTION

The ADD8733 is a 4-channel regulator with two VCOM amplifiers and gate pulse modulation (GPM) that provides all the necessary voltages for thin film transistor (TFT) liquid crystal displays (LCD). Included is a step-up regulator, a step-down regulator for digital logic, two VCOM amplifiers, two charge-pump regulators for VGH and VGL, and an integrated gate pulse modulator.

By offering a complete power integration solution optimized for TFT LCD TVs and monitors, the ADD8733 helps to lower cost, simplify board design, and increase performance over existing solutions.

The ADD8733 is offered in a 48-lead RoHS compliant LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

Rev. PrA

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SPECIFICATIONS

STEP-UP SWITCHING REGULATOR SPECIFICATIONS

V_{VIN} = V_{SD_VIN} = 12 V, L1= 15 µH, T_A = 25°C, f_{OSC} = 650 kHz, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Input Voltage	VIN		8.0		16.5	V
Maximum Duty Cycle				70		%
OUTPUT						
Output Voltage	V_{SU_OUT}		VIN + 1		20	V
Load Regulation		200 mA ≤ I_{LOAD} ≤ 800 mA, V_{SU_OUT} = 18 V		1		%
Line Regulation		I_{LOAD} = 500 mA, 8 V ≤ V_{SD_VIN} ≤ 16.5 V, V_{SU_OUT} = 18 V		1		%
Overall Regulation		Line, load, temperature			±3	%
Overvoltage Protection	V_{SU_D}		19.5	20	20.5	V
REFERENCE						
FB Regulation Voltage	V_{SU_FB}			2.5		V
ERROR AMPLIFIER						
Transconductance	g_m			100		µA/V
Error Amplifier Open-Loop Voltage Gain	A_{VSU}			1000		V/V
Input Bias Current	I_B			100		nA
SWITCH						
On Resistance	$R_{DS\ (ON)SU}$			100		mΩ
Peak Current Limit	$I_{SUCLSET}$			3		A
OSCILLATOR						
Oscillator Frequency	f_{OSC}	FREQ = GND		650		kHz
		FREQ = VSR_OUT[1]		1200		kHz

[1] VSR_OUT pin provides a logic-high output of 5 V.

STEP-DOWN REGULATOR SPECIFICATIONS

V_{VIN} = V_{SD_VIN} = 12 V, L2=10 µH, T_A = 25°C, f_{OSC} = 650 kHz, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Input Voltage	V_{SD_VIN}		8.0		16.5	V
Minimum Duty Cycle				15		%
OUTPUT						
Output Voltage	V_{STEP_DN}		2.5		5	V
Load Regulation		500 mA ≤ I_{LOAD} ≤ 1000 mA, V_{STEP_DN} = 3.3 V		1		%
Line Regulation		I_{LOAD} = 750 mA, 8 V ≤ V_{SD_VIN} ≤ 16.5 V, V_{STEP_DN} = 3.3 V		1		%
Overall Regulation		Line, load, temperature			±3	%
ERROR AMPLIFER						
FB Regulation Voltage	V_{SD_FB}			2.5		V
FB Input Bias Current	I_{SD_FB}			TBD		nA
Error Amplifier Open-Loop Voltage Gain	A_{VSD}			TBD		V/V
COMP Output Current	I_{SD_COMP}			TBD		µA
SWITCH						
On Resistance	$R_{DS\ (ON)SD}$	SD_BS = 5 V, I_{SD_LOAD} = 750 mA		100		mΩ
Peak Current Limit	$I_{SDCLSET}$			3		A
OSCILLATOR						
Oscillator Frequency	f_{OSC}	FREQ = GND		650		kHz
		FREQ = VSR_OUT[1]		1200		kHz

[1] VSR_OUT pin provides a logic-high output of 5 V.

POSITIVE CHARGE-PUMP REGULATOR SPECIFICATIONS

V_{NPCP_SUP} = 12 V, T_A = 25°C, f_{OSC} = 650 kHz, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
SUPPLY					
Supply Voltage	V_{NPCP_SUP}	8		20	V
OUTPUT					
Output Current	I_{VGH}		50		mA
REFERENCE					
FB Regulation Voltage	V_{NPCP_FB}		2.5		V

NEGATIVE CHARGE-PUMP REGULATOR SPECIFICATIONS

V_{NPCP_SUP} = 12 V, T_A = 25°C, f_{OSC} = 650 kHz, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
SUPPLY					
Supply Voltage	V_{NPCP_SUP}	8		20	V
OUTPUT					
Output Voltage	V_{GL}	$(-V_{NPCP\_SUP} + 3)$		−2	V
Output Current	I_{VGL}		70		mA
REFERENCE					
Reference Voltage	V_{NCP_REF}		2.5		V
FB Regulation Voltage	V_{NCP_FB}		0		V

GATE PULSE MODULATOR SPECIFICATIONS

V_{SD_VIN} = 12 V, V_{GPM_H} = 28 V, V_{GPM_L} = 12 V[1], T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
GPM_H Voltage	V_{GPM_H}		GPM_L + 6		30	V
GPM_H Input Current	I_{GPM_H}	GPM_FLK = GND, GPM_DPM = logic high		TBD		µs
GPM_L Voltage	V_{GPM_L}		5		GPM_H – 6	V
GPM_L Input Current	I_{GPM_L}	GPM_FLK = GPM_DPM = logic high		TBD		µs
CONTROL INPUT CHARACTERISTICS						
GPM_FLK Voltage Low	V_{LOWFLK}				0.8	V
GPM_FLK Voltage High	$V_{HIGHFLK}$		2.2			V
GPM_FLK Input Current	I_{GPM_FLK}	0.9 V ≤ GPM_FLK ≤ 3.3 V	−1		+1	µA
GPM_DPM Voltage Low	V_{LOWDPM}				0.8	V
GPM_DPM Voltage High	$V_{HIGHDPM}$		2.2			V
GPM_DPM Input Current	I_{GPM_DPM}	0.9 V ≤ V_{GPM_DPM} ≤ 3.3 V	−1		+1	µA
SWITCHING CHARACTERISTICS						
GPM_OUT Discharge Current	I_{GPM_OUT}	RE = 400 Ω , GPM_L = 12 V		30		mA
DELAY CHARACTERISTICS						
Delay Time	t_{DELAY}	CE = 470 pF		TBD		µs

[1] Refer to Figure 6 in the Typical Application Circuit section.

VCOM AMPLIFIER SPECIFICATIONS

V_{SU_S} = 12 V, VCx_POS = 6.0 V, T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			TBD		mV
Noninverting Input Bias Current	I_B			50	300	nA
Input Voltage Range			2		SU_S – 2	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 2 V to (SU_S – 3) V		60		dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (High)	V_{OH}	Buffer, I_{VC_OUT} (source) = 100 µA		SU_S – 0.08		V
Output Voltage Swing (Low)	V_{OL}	Buffer, I_{VC_OUT} (sink) = 100 µA		30		mV
Output Current Limit	I_{OUT}			±250		mA
POWER SUPPLY						
Supply Voltage	V_{SU_S}		8		20	V
Power Supply Rejection Ratio	PSRR	7.5 V ≤ SU_S ≤ 20.5 V	65	70		dB
Supply Current[1]	I_{SY}	No load, VCx_POS = SU_S/2		2		mA

[1] Supply current for one VCOM amplifier.

GENERAL SPECIFICATIONS

V_{VIN} = V_{SD_VIN} = 12 V, T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Applied Input Voltage (VIN)	V_{VIN}		8		16.5	V
UNDERVOLTAGE LOCKOUT						
Rising Input Voltage (VIN)	V_{UVLOR}	TBD		7.5		V
Falling Input Voltage (VIN)	V_{UVLOF}			7.2		V
THERMAL PROTECTION						
Thermal Shutdown		Rising temperature		145		°C
Thermal Shutdown		Falling temperature		105		°C
SERIES SWITCH						
On Resistance	$R_{DS\ (ON)SSW}$			200		mΩ
Peak Current	I_{SSWPKC}				TBD	mA

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter[1]	Rating
SD_VIN/SD_SW/SD_BS/SD_FB/SD_COMP to SU_PGND	TBD
NCP_REF/NCP_FB/NCP_DRV to NPCP_GND	TBD
PCP_FB/PCP_DRV/NPCP_SUP to NPCP_GND	TBD
GPM_FLK/GPM_CE/GPM_DPM to GND	TBD
GPM_RE/GPM_OUT/GPM_H/GPM_L to GND	TBD
VC1_POS/VC1_NEG/VC1_OUT/VC2_OUT/VC2_POS/ VC2_NEG to VC1_GND	TBD
SU_SW/SU_D/SU_S/SU_FB/SU_COMP to SU_PGND	TBD
VGL_DLY/SU_DLY/SD_SS/SU_SS/VSR_OUT to GND	TBD
Voltage Between SU_PGND, NPCP_GND, and GND	±0.5
Package Power Dissipation (P_D)	$(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance for Exposed Pad Soldered to 4-Layer JEDEC PC Board (θ_{JA})	25.88°C/W
Maximum Junction Temperature (T_J)	125°C
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Reflow Peak Temperature (20 sec to 40 sec)	250°C

[1] SU_PGND, VC1_GND, NPCP_GND, and GND are connected to a common ground connection.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

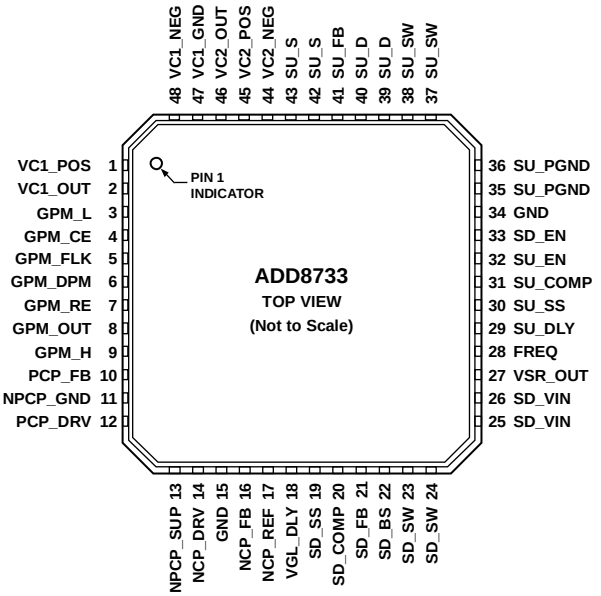

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Function	Description
1	VC1_POS	Input	VCOM Amplifier 1 Positive Input
2	VC1_OUT	Output	VCOM Amplifier 1 Output
3	GPM_L		Low Level Voltage for Gate Pulse Modulation
4	GPM_CE		Capacitor Programmable FLK to Falling Slope Delay
5	GPM_FLK	Input	Control Pin for Gate Pulse Modulation
6	GPM_DPM	Input	Control Pin for Gate Pulse Modulation (On/Off)
7	GPM_RE		Resistor Programmable Gate Pulse Modulation Falling Slope
8	GPM_OUT	Power Out	V_{GH}/Gate Pulse Modulation Output
9	GPM_H	Power In	High Level Voltage for Gate Pulse Modulation
10	PCP_FB	Input	Positive Charge Pump Feedback
11	NPCP_GND	GND	Positive and Negative Charge Pump Ground
12	PCP_DRV		Positive Charge Pump Capacitor Drive
13	NPCP_SUP	Power In	Positive and Negative Charge Pump Power In
14	NCP_DRV		Negative Charge Pump Capacitor Drive
15	GND	GND	Voltage Subregulator Ground Pin
16	NCP_FB	Input	Negative Charge Pump Feedback
17	NCP_REF		Negative Charge Pump Reference
18	VGL_DLY		Delay for Step-Down
19	SD_SS		Soft Start for Step-Down
20	SD_COMP		Step-Down Regulator Compensation
21	SD_FB	Input	Step-Down Regulator Feedback
22	SD_BS	Input	Step-Down Regulator Bootstrap Driver Power Input
23, 24	SD_SW		Step-Down Regulator Switch Node
25, 26	SD_VIN	Power In	Power VIN for Step-Down Regulator's High Side Switch
27	VSR_OUT		Voltage Subregulator Output Voltage
28	FREQ		Frequency Select
29	SU_DLY		Delay for Step-Up
30	SU_SS		Soft Start for Step-Up
31	SU_COMP		Step-Up Regulator Compensation

Pin No.	Mnemonic	Function	Description
32	SU_EN		Step-Up Enable for Power Supply Sequencing
33	SD_EN		Step-Down Enable for Power Supply Sequencing
34	GND	GND	Ground Pin
35, 36	SU_PGND	GND	Ground Pin for Step-Up
37, 38	SU_SW		Step-Up Regulator Switch Node
39, 40	SU_D	Power In	Power In for Step-Up Regulator Power Supply Sequencing Switch
41	SU_FB	Input	Step-Up Regulator Feedback
42, 43	SU_S	Power Out	Output from Step-Up Regulator Power Supply Sequencing Switch
44	VC2_NEG	Input	VCOM Amplifier 2 Negative Input
45	VC2_POS	Input	VCOM Amplifier 2 Positive Input
46	VC2_OUT	Output	VCOM Amplifier 2 Output
47	VC1_GND	GND	Ground Pin for VCOM Amplifier 1
48	VC1_NEG	Input	VCOM Amplifier 1 Negative Input

TIMING DIAGRAMS

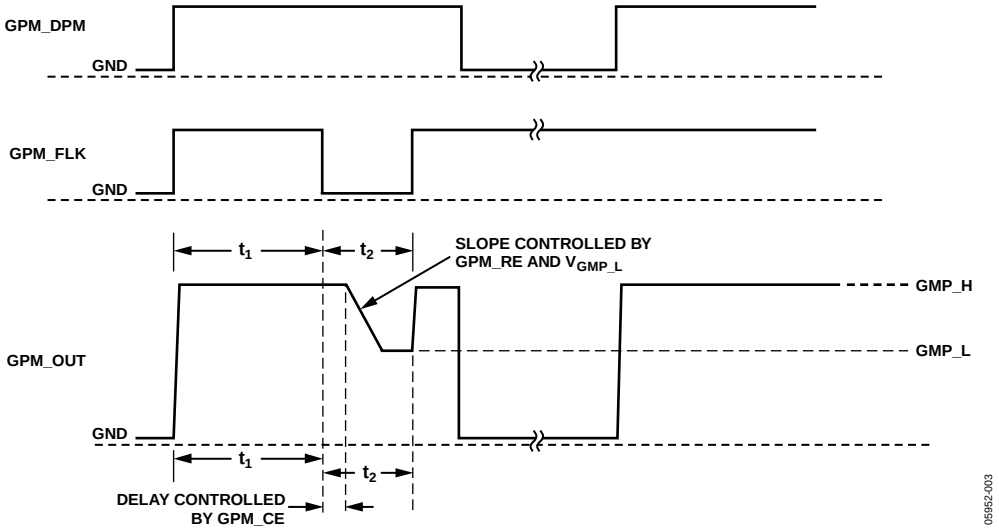

Figure 3. Timing Diagram for Gate Pulse Modulator

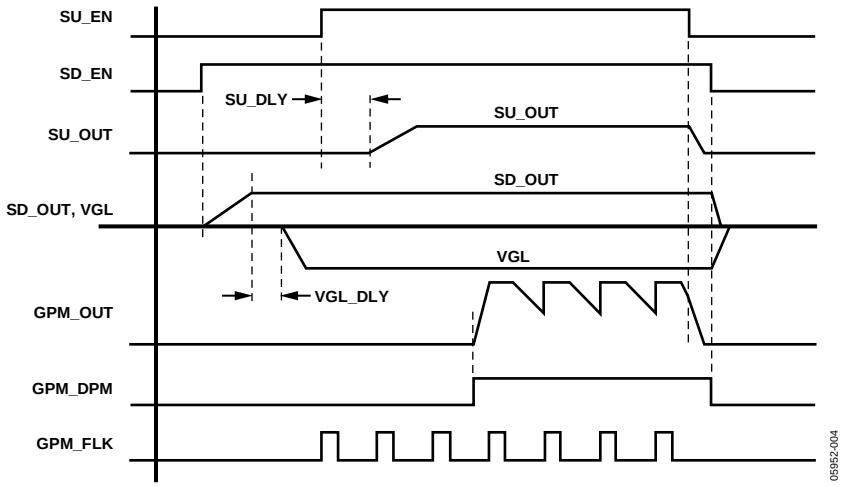

Figure 4. Timing Diagram for Power-Up Sequence 1

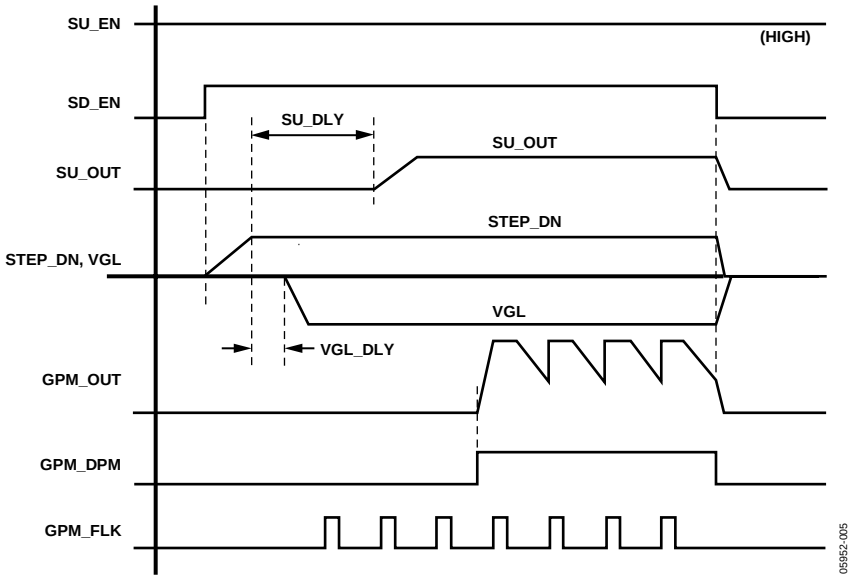

Figure 5. Timing Diagram for Power-Up Sequence 2

TYPICAL APPLICATION CIRCUIT

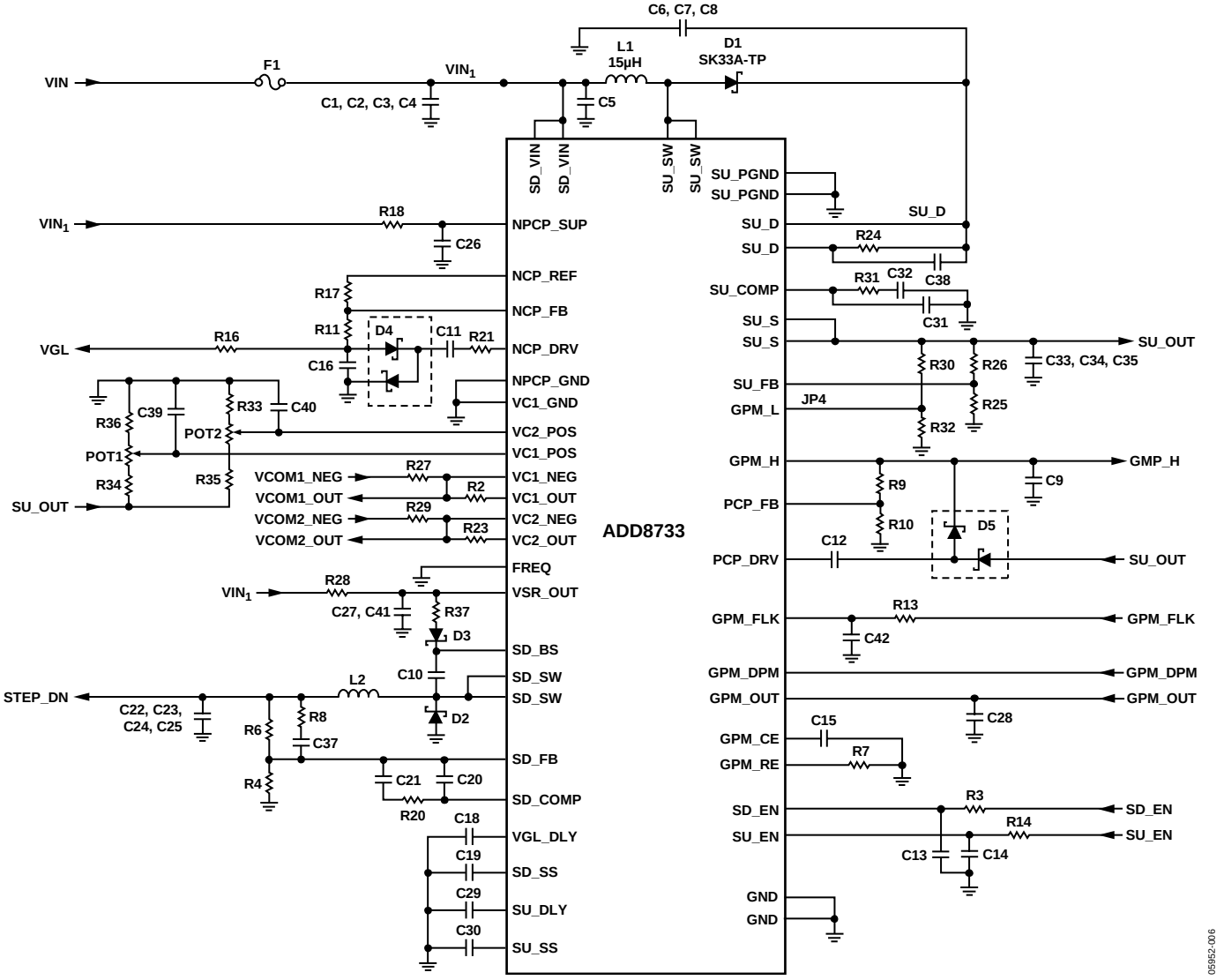

Figure 6. Typical Application Circuit with Component Variables, 650 kHz

LAND PATTERN

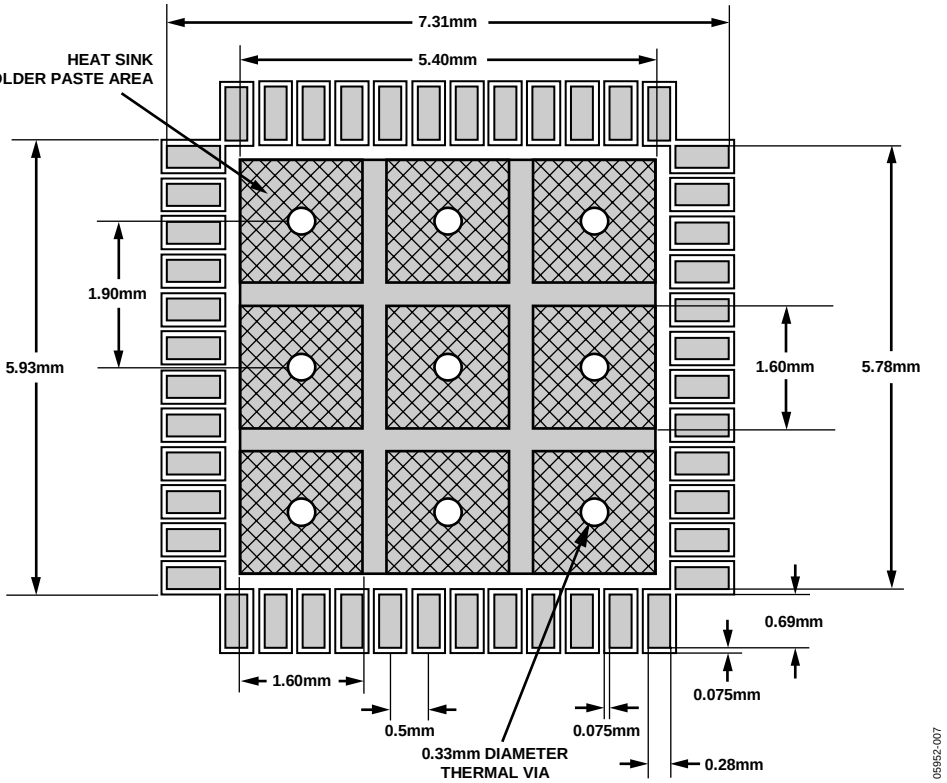

Figure 7. 48-Lead LFCSP (CP-48-1) Land Pattern

OUTLINE DIMENSIONS

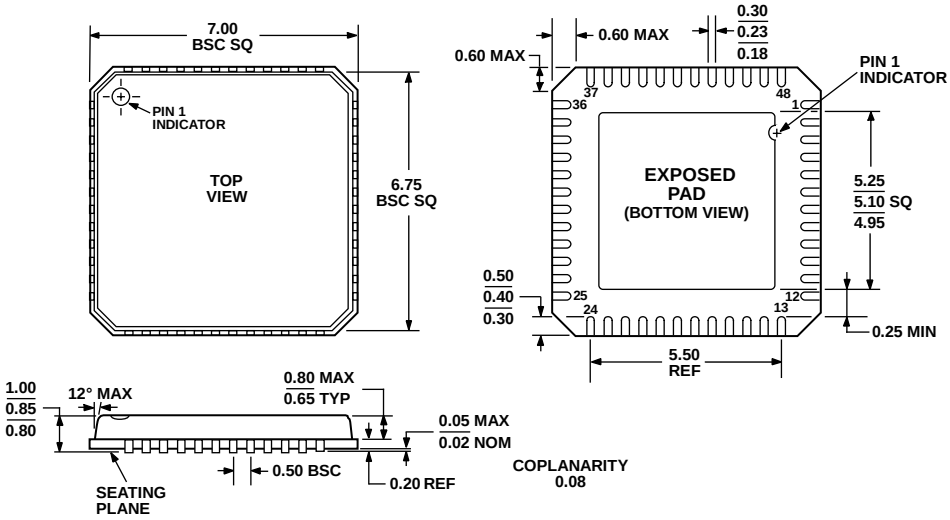

Figure 8. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADD8733ACPZ-REEL[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-1

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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